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09/901,740	07/09/2001	Robert Rogenmoser	5580-03100	8445
34399	7590 02/11/2004		EXAMINER	
GARLICK HARRISON & MARKISON LLP			CUNNINGHAM, TERRY D	
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- ,			2816	

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Please find below and/or attached an Office communication concerning this application or proceeding.

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Paper No(s)/Mail Date _

Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)

6) U Other:

Art Unit: 2816

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-9 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 4-5, the phrase "corresponding to selecting one of the first plurality of inputs signals as output" is not understood. It is not seen possible that "signals" can <u>correspond</u> to "selecting". It is suggested that this phrase be changed to --and selecting one of the first plurality of inputs signals, responsive to the first plurality of select signals, as output--. Lines 16-17 are rejected for similar reasons as lines 4-5. In line 23, it is deemed inappropriate to use the phrase "one of" with the conjunction "or". It suggested that "one of' be changed to --either-- or "or" be changed to --and--.

Claims 2-9 and 11 are rejected for the reasons discussed above with claim 1.

In claim 3, there is no support found for the recited elements in addition to the structure of claims 1 and 2. As clearly understood from the specification, the elements recited in claim 3 are part of each the "first passgate circuit" and the "second passgate circuit" and should be recited as such".

With respect to claim 3, Examiner points output that Applicant remarks that claim 2 claims "a default circuit with multiple passgate circuits". However, there is no support found for the "default circuits" having "multiple passgate circuits". Examiner further points out that no

Art Unit: 2816

indefiniteness rejection have been made because the claim fails to recite that the "first" and "second plurality of passgate circuits" are part of any already recited element.

In claim 4, the language therein is not understood because "NAND logic" is operation a circuit cannot comprise operation. It is suggested that either "comprises" be changed to --performs-- or that "logic" be changed back to --gate--.

Claim 6 is rejected for similar reasons as claim 4.

Claim 7, lines 3-4 are deemed indefinite for similar reasons as claim 1, lines 4-5.

Claim 8 is rejected for similar reasons as claim 3.

In claim 11, line 1, it is noted that "drive" should be changed to --driven--

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. §102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless —

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5 and 7-9 are rejected under 35 U.S.C. §102(b) as being anticipated by Béchade (USPN 5,789,966 - cited by Applicant). Béchade discloses, in Fig. 2, a circuit comprising: "a first plurality of passgates (I0 and I1)"; "a first circuit (22 and 28) in 20')"; "a second plurality of passgates (I2 and I3)"; "a second circuit (22 and 28 (28 not shown, but disclosed) in 20'')"; and "a third circuit (24 and 26)", all connected and operating similarly as recited by Applicant.

With respect to claim 7, it is clear from the reference to Béchade, particularly from the claims, that any number of passgate circuits is intended.

Art Unit: 2816

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 6 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Béchade.

With respect to claim 6, the above discussed circuit to Béchade does not expressly disclose using a "NOR gate". However, it is notoriously well known in the art to manufacture an OR gate, as shown for 28, using a NOR gate and an inverter. Such a structure is known to have simple construction with low threshold loss. Therefore, it would have been obvious for one skilled in the art to use a NOR gate with an inverter for OR gate 28 of Béchade to obtain the expected advantage of simple construction with low threshold loss.

With respect to claim 11, the above-discussed circuit to Béchade does not expressly disclose using a PMOS transistor. However, it is notoriously well known that NMOS transistor and PMOS transistors with an inverter on the gate are art-recognized. Therefore, it would have been obvious for one skilled in the art to use a PMOS transistor with an inverter on the gate for NMOS 22 of Béchade due to the doctrine of equivalents.

Examiner has fully considered Applicant's remarks for the above rejection and has not found them to be persuasive. Applicant remarks that "Bechade fails to disclose multiplexing multiple bits per input". However, this statement is not at all understood. The claims do not state anything similar to this remark. Nowhere does the claim discuss any "bits". This claim

recites that the each "passgate circuit" select one of the "input signals" responsive to the "select signals". This is exactly what the reference to Béchade is doing.

Applicant further remarks "as recited in claim 3, Bechade fails to disclose the use of a default circuit with multiple passgate circuits". Again this remark is not understood. Claim 3 does not recited that the "default circuit" has "multiple passgate circuits", it only recited that it is "coupled to" the "passgate circuits".

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Terry Cunningham whose telephone number is 571-272-1742. The examiner can normally be reached on Monday-Thursday from 7:30 to 6:00.

Art Unit: 2816

Page 6

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy P. Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is 703-308-0956.

TC February 9, 2004 Terry D. Cunningham Primary Examiner Art Unit 2816